AMENDMENTS TO THE SPECIFICATION

IN THE SPECIFICATION

Please amend the paragraph on page 1, line 14 as follows:

An apparent paradox of today's semiconductor based data processing devices is that although the performance of the microprocessors as an average has increased by 60% per year in recent times and hence increased ~~with a factor on~~ about 100 fold from the end of the eighties and up to 1998, the access time of random accessible write/read memories, so-called RAMs has diminished at ~~with~~ about 7% per year and hence only been halved in the same time period. The gap between processor performance and the access bandwidth of RAMs has hence increased by ~~with~~ a factor of about 50 during the last ten years. The development in regard of processor performance and access time hence makes it necessary to improve both the memory bandwidth and reduce the latency, that is the waiting time which occurs when instructions and data ~~shall be~~ a re fetched. The emphasis in the development of dynamic RAMs (DRAMs) has, however, been on reducing the size of the memory cells in order to realise DRAMs with high storage density.

Please amend the paragraph on page 1, line 28 as follows:

Generally, however, the cause of the above misproportion is quite evident. The processor must communicate with one or more memory types during the

different phases of a computing task and in some cases the communication will be very intensive, for instance when the processing presupposes the use of look-up tables. In order to achieve high processing speeds, the fastest and most commonly used memories are provided physically integrated with the central processing unit. Unfortunately, such memories consume a relatively large chip area if their storage capacity is to ~~shall~~ be sufficient and it is necessary ~~with an unfortunate~~ to compromise in order to distribute the available physical area between processor and high-speed memories. This in its turn implies that further memory capacity only can be obtained via bus lines to more distant memory units. Depending on an optimisation in each separate case, the result will generally be that a total device architecture is obtained where much of the chip area and the processing performance of the central processing unit are used for handling the data flow between the central processing unit and more distant memory units which are connected with the central processing unit via bus lines on the semiconductor substrate.

Please amend the paragraph on page 2, line 10 as follows:

In concrete terms this means that the microprocessor uses 75% of its time in the memory device when it ~~shall~~ executes database processing and matrix computations. The development has been such that 60% of the area and 90% of the transistors of the most modern microprocessors are adapted to handle the gap between the processor performance and access bandwidth by being used in

special hardware on the chip, for instance in special high-speed memories or cache memories in order to handle the increasing latency. Also in regard of dynamic RAM (DRAM), ~~has~~ the development caused unexpected difficulties. In 1986 it was employed a typical minimum memory capacity for PCs of 32 1 Mbit DRAM, while it in 1997 was used two 64 Mbit DRAMs because the growth rate of the minimum memory size only was half of the growth rate of the capacity of the DRAM. As most of today's microprocessors are oriented towards the use of cache memories, it is necessary with lower latency, but the development has instead progressed towards the higher bandwidths and high latency. It is evident that simply increasing the capacity of the DRAMs will not be satisfactory ~~be no solution~~, as DRAMs with a capacity of 256 Mbit or 1 Gbit in reality ~~shall~~ results in higher costs per bit and cause a higher bandwidth requirement for error control. If the latter is to be met, the latencity, however, will be correspondingly higher.

Please amend the paragraph on page 2, line 29 as follows:

In order to solve the problems which the disproportion between the processor performance and a RAM access time causes, it has recently been proposed (Patterson & A1., "Intelligent RAM (IRAM): Chips that Remember and Compute", 1997 IEEE International Solid-State Circuits Conference, pp. 224-225) to implement processing logic and memory on one and the same chip, where most of the transistors will be used in the memory device. An integrated

data processing device of this kind has been denoted intelligent RAM or IRAM. The use of a DRAM with 1 Gbit capacity provides enough transistors to implement a powerful processor and a memory which is large enough to contain whole programs and data sets. In an IRAM of this kind, the memory is divided into blocks with memory gates with a width of for instance 1 Kbit. Typical chip sizes will be 600 mm^2, such that an IRAM ~~shall need~~ requires more metal layers in order to increase the transmission speed of the lines and possibly also require faster transistors for the high-speed interface of synchronous DRAMs. The possible advantages suggested in case of IRAM include lower memory latency, e.g reduced by a factor of 10^{-1}, high memory bandwidth, for instance any increase with a factor of 100, and lower power consumption. The dimensions of the memory (width dimension) can be adjusted, and an IRAM should ~~shall~~ not occupy an area on the board as large as conventional data processing devices with corresponding capacity in regard of storage and processing would do.

Please amend the paragraph on page 3, line 14 as follows:

Alternatively it has been suggested (Yoo & al., "A 32-bank 1 Gb DRAM with GB/s Bandwidth, ISSCC Digest of Technical Papers, pp. 378-379, Feb. 1996) to employ IRAM with vector processors. Such vector processors work with linear number arrays. Vector processors do not need cache memories, but require memory with low latency, often realized as static RAM (SRAM) ~~eg~~ with large bandwidth, as hundreds of separate memory groups may be used. The

proposed IRAM system with a memory capacity of 1 Gbit will hence be adapted to the needs of a vector processor. This prior art is shown in figure 1 which schematically suggests how an IRAM vector microprocessor may be realized. Based on a 0.18 μ DRAM process with a chip area of 6 cm^2 an IRAM could have 16 addition and multiplication units with a frequency of 500 MHz collectively to ~~would~~ provide 100 Gbyte/s memory bandwidth. An IRAM of this kind could execute a typical test program (Linpack) with a speed of 8 GFLOPS, which is five times faster than Cray's ~~fasters~~ vector-based supercomputer processor (Cray T-90). Whether IRAMs may have a breakthrough will be dependent on the memory capacity on a chip, as this is expected to increase from 10-32 Mb for graphic products such as games and to 128-256 Mb for network computers and portable PCs.

Please amend the paragraph on page 3, line 33 as follows:

Further, ~~there are in the art also known~~ the use of parallel processing in order to increase the processing speed is also known in the art. This has been achieved by basing the processors on architectures which allows processing of data and data sets in parallel. Typical examples are parallel processors on instruction level such as pipeline processors or superscalar which have an architecture that ~~which~~ can handle very long instruction words (VLIW). ~~It has also been developed~~ Also, processors have been developed, which works on instruction level, but with data in parallel, and this may be realized either with

pipeline architectures, systolic architectures, and, as mentioned above, with vector architectures. A difficult realizable desired goal has been the development of data processing devices which can work with architectures which allows parallel data processing on process level, that is so-called MIMD architectures (Multiple Instructions, Multiple Data). ~~It has been proposed~~ MIMD architectures with either distributed memories or common memories have been proposed, but in practice most of these architectures are initially based on different forms of multiprocessing in parallel, that is with use of processor networks. This is currently ~~today~~ difficult to realize with an optimal interconnectivity and in ~~is~~ any case impossible to implement in a chip configuration with current ~~today's~~ semiconductor technology, particularly as long as the chip size is limited to a few cm^2.

Please amend the paragraph on page 4, line 16 as follows:

The increasing gap between the theoretical processing speed of modem central processing units and the total speed of the device is an important problem which has provided to be very difficult to overcome ~~obviate~~ and almost impossible to solve by a further development of data processing devices based on for instance silicon-based semiconductor technology only. Neither an increase in chip size or structural solutions which employ vertical structures and hence achieve more components on one and the same substrate material have turned out to be suitable. This is closely connected with the memory devices comprising

memory cells which explicitly are dependent on switches implemented in the semiconductor material of the substrate. In other words, each bit spot in a memory must have exclusive access to a part of the substrate, and hence structural solutions are required wherein memory devices and processor must be provided in juxtaposition. Attempts to form vertical structures, for instance by stacking several layers on each other, have also failed because it is still necessary to provide ~~with the~~ electrical access and components, for instance switches, in the same underlying semiconductor substrate~~,~~. Hence no net capacity increase is obtained by use of multilayer solutions and with the substrate area already exploited with maximum density. By using vertical stacked circuit layers ~~it additionally becomes a problem with the~~ heat dissipation of ~~in~~ the separate layers also becomes a problem, as today's semiconductor-based memories are volatile and hence need ~~a~~ refresh current, which generates heat.

Please amend the paragraph on page 7, line 15 as follows:

Further there may be ~~as instance of prior art be mentioned~~ a number of patent publications which have a certain generic relation to the last-mentioned US patent no. 5 702 963 as they concern circuit structures in two or three dimensions and substantially made in conventional semiconductor technology.

Please amend the paragraph on page 12, line 21 as follows:

According to the invention ~~can advantageously~~ the ~~further~~ electrical conducting structures can advantageously be provided as electrical edge connections on or cover at least one side of one or more main layers in order to contact electrical conducting structures in other main layers and/or provide electrical connection between main layers and substrate, and/or also be provided as vertical conducting structures in one or more main layers and form electrical connections in the cross-direction of the main layers and perpendicular to their planes in order to contact electrical conducting structures in other main layers and/or to provide electrical connection between the main layers and substrate.

Please amend the paragraph on page 16, line 23 as follows:

Fig. 3 shows more explicitly a first embodiment of the data processing device according to the invention and substantially realized on the first level of the functional hierarchy. Here once again the processor layer P is provided on a substrate S and will as before include active components such as transistors in order to realize one or more central processors and possible control and communication processors. Above the processor layer P a memory interface 1 is provided and extends beyond the processor layer P and over the substrate S. Above the memory interface memory layers M_1, M_2 . . . are provided. Both the

processor layer P and the memory layers M and memory interface 1 comprise ~~not shown~~ horizontal electrical conducting structures (not shown) to provide connection between the separate components, but in addition these conducting structures are in the memory layers M conveyed to electrical edge connections at the side of the memory layer and the memory buses 2 which are provided in a separate memory bus module 2' as shown in the figure. For each memory layer M_1, M_2 . . . there are provided corresponding memory buses 2_1, 2_2 . . . and they may in their turn be generated as both horizontal and vertical electrical conducting structures in the memory bus module 2'.

Please amend the paragraph on page 19, line 34 as follows:

Above the memory layer M_3 a memory interface 1 is provided and above this follows further memory layers M_4, M_5 . . . in a very large number and there may well realize a mass memory in the data processing device. These further memory layers M_4, M_5 as via memory buses 2 realized in the form of vertical electrical conducting structures, conveyed to the memory interface 1. Correspondingly are the separate RAM in the memory layers M_1, M_2, M_3 also conveyed to the memory interface 1 ~~hrough~~ through the separate layers extending via vertical memory buses 2. In addition memory buses 7 which lead to the I/O ports on the separate RAMs are provided between the processors 5 in the processor layers P_1, P_2, P_3 and assigned RAM in the memory layers M_1, M_2, M_3. For each processor 5 two such memory busses 7 are drawn for symbolically

to indicate separate instruction and data buses. This is of course no condition. The processor interface 3 is connected to possible external units over an I/O-bus 8 and correspondingly an I/O-bus 9 is provided for the memory interface 1.

Please amend the paragraph on page 23, line 12 as follows:

In ~~I~~ NO patent application 972803 which has been assigned to the present applicant and which hereby is incorporated as reference, there is disclosed an electrically addressable logic device suitable for storage or processing of data. An embodiment of this device configured as a data memory is shown in fig. 7a. The memory comprises a memory medium 10 which forms a layer-like continuous structure which can be realized as a layer in one of the memory layers M in the present invention. The memory medium 10 is formed by a substantially organic material which may go through a physical or chemical change of state by a suitable energetic influence. The memory medium 10 is as shown in fig. 7a provided between a matrix of substantially orthogonal intersecting electrodes 11 and 12 such that these in relation to the memory medium form a substantially orthogonal electrode matrix which everywhere contacts the memory medium directly. It is to be understood that electrodes 11, 12 may be realized as the above-mentioned conducting structures in a memory layer M. In the intersection between an underlying electrode 11 and an overlying electrode 12 there is in the memory material 10 formed a logic cell which under influence of voltage, current or an electric field may attain a state which can represent the

predetermined logic value of the cell. The logic cells hence constitute the memory elements in the memory as shown in fig. 7a. Each of the electrodes 11, 12 is connected with a memory bus module 2' via addressing lines 13 and the memory bus module is over the memory bus 2 connected with a memory interface 1 which may be provided in another layer in the data processing device and spaced apart from the memory layer in question, the memory bus 2 for this purpose partly being embodied as vertical conducting structures which extend through the different layers in the data processing device, as this schematically is indicated in fig. 7b which shows a section through the memory in fig. 7a taken along one of the electrodes 12. Fig. 7c and 7d show sections through the separate memory cell 14 which is formed in the intersection between an overlying electrode 11 and an underlying electrode 12. It is to be understood that the electrodes 12 and 11 may be provided in or on the memory medium 10 and contact this directly or there may on both sides of said memory medium be provided not shown dielectric layers, such that the electrodes 11, 12 contact the memory medium 10 indirectly. If a voltage is applied to the electrodes 11, 12 a direct or indirect electrical connection are in each case obtained through the memory element, such that it may be brought to definite state or that a definite state in the memory element 14 may be detected. The change of state in the memory element 14 may be a change in the current or voltage characteristics of the memory material in this location or a change in the impedance value of the

material. By selecting suitable materials a specific state in absence of voltage or electrical fields will be permanent such that the state is maintained permanently and the memory in fig. 7a hence realizes a non-volatile electrically addressable memory device. The memory material itself may be a polymer, material, for instance a conjugated polymer and it may also comprise an anisotropic electrical conducting material, that is a material which only conducts electricity in the transversal direction between the electrodes, such that in the memory material electric currents which propagate in the longitudinal direction are not generated. The memory material 10 may also be realized in this way or added substances which under the influence of voltage or electric fields cause it to transfer from a crystalline into an amorphous phase or vice versa, the current/voltage characteristics of the phase state being distinct and allowing a detection. The electrodes 11, 12 which are realized in the form of horizontal conducting structures in the memory layer M in question may in themselves be a conducting organic material and be realized in form of the deposited metal-organic compounds or as metals on the surface 10 of the memory material. Further the memory element or the logic cell 10, 14 may realize a rectifying diode between the electrodes 11, 12 such that the memory device in fig. 7a forms an electric network of such diodes. The consequence of this shall be described more closely in the following, but a diode network of this kind may prevent write and/or detection errors due to sneak currents from a memory element to another in the

electrode matrix. Particularly, there may be used an organic memory material 10 which spontaneously forms a diode junction in the memory element 14. Further it is regarded as advantageous that the logic cell is realized such that the memory material 10 under influence of electric currents or electric fields undergoes a reaction which causes the resistance value of the separate logic cell to change. Then the value of the logic cell may be detected by measuring the impedance of a logic cell, and this detection of course corresponds to a reading of the content of the memory device as shown in fig. 7a. If the logical value of the memory element can be switched reversibly, the memory device in fig. 7a realizes a write/read memory or memory of the ERASABLE type, but there is nothing against that the logic value may be switched irreversibly, such that the memory device in fig. 7a thus realizes a read only memory (ROM) or a memory of the type WORM. By using a memory device as shown in fig. 7a in the form of stacked memory layers M, these must be mutually isolated and this can take place by providing dielectric thin layers 15 on each side of the electrodes. If the electrodes now 11, 12 now are located on the surface of the memory material, they may simultaneously be incorporated in these dielectric layers 15 as shown in fig. 7d.

Please amend the paragraph on page 28, line 15 as follows:

The structure in fig. 9 allows a direct detection of the conductivity state of the functional element 17 on the basis of the current/voltage characteristics of the means. The electrode means as shown in fig. 8 may be used in an electrical

addressable logic device, particularly a passive addressable memory device, such this is shown schematically realized in fig. 10. A plurality of electrodes 11, 12 are provided such that they form a substantially orthogonal matrix of x,y electrodes and with the electrode means in fig. 8 in each intersection of the electrodes. When the electrode means are realized with the structures as shown in fig. 9, there is at each intersection between an x electrode and an y electrode obtained a diode 13 which in each case has the same conduction direction. It is also possible that the separate electrode means may be realized with an inherent rectifying function. This rectifying function is necessary to avoid cross-talk problems in addressing the electrode means used in a passive matrix as shown in fig. 10. A selective addressing of the separate electrode means namely requires that in each electrode means there must be a rectifying contact, for instance as mentioned between the underlying electrode 11 and a contact layer 16. When a functional element 17 in x,y position in the matrix shall be addressed, there must be no current transfer at adjacent intersections (x+1,y), (x-1,y), (x,y+1) or (x,y-1). It shall in this connection be understood that diodes 18 in fig. 10 only constitute an equivalent model of the rectifying function of the electrode means in the intersection between the electrodes 11, 12.

Please amend the paragraph on page 29, line 22 as follows:

Electrode means as shown in fig. 8 may also generally be used as a logic device in the data processing device according to the invention. This

presupposes that the functional element 17 in each electrode means is adapted such that it can be switched from a state to another, possibly between several states and hence be used for realizing logic gates or logic networks. The same condition will of course be present if the device shown in fig. 10 ~~shall be~~ is used for realizing a RAM or a memory of the type ERASABLE. ~~Purely practically~~ Practically ~~can~~ the device disclosed in NO patent application 973390 can be used for realizing a memory device with an order of magnitude of 1 cm^2 and wholly in a thin-film technology. The separate memory elements may then be made as small as practically possible to attain with patterning methods for electrodes, contact layers and functional elements. - In principle ~~there would be nothing against that~~ the material in the contact layer ~~was an~~ can be isotropic conducting material, but this is based on the condition that the contact layer is thin and that at the distance between the electrode means, that is the intersection between the electrodes 11, 12 in the matrix in fig. 10, is large. - If it is desirable with the high storage density in a memory device realized as shown in fig. 10, the extension of the electrode means as shown in fig. 8 will be small and the intersections in the electrode matrix be located very close to each other. It is then becomes advantageous to use ~~an obvious advantage using~~ an anisotropic conducting material, particularly a polymer material, in the electrode means in fig. 8.

Please amend the paragraph on page 30, line 7 as follows:

Finally, ~~it shall be mentioned that~~ the contact layer also may be realized with non-linear current/voltage characteristics and made in a semi-conducting organic material, for instance a semi-conducting polymer. With the structure shown in fig. 9 as a starting point it will then be possible to realize the electrode means in fig. 8 with a transistor function. This ~~shall not be discussed in further detail here, but~~ will be <u>further discussed</u> ~~mentioned in the following~~ in connection with the discussion of transistors which may be used for realizing active components in the processing unit and the storage unit in the data processing device according to the present invention. In the above there is in connection with the discussion of fig. 7-10 substantially presupposed that the means shown therein <u>can</u> ~~shall~~ be used for realizing information storing functions, that is realized as memories in the storage unit. It is, as already mentioned, ~~nothing against that~~ they may be used for realizing logic devices generally, if the logic material or the active material used between the electrodes can be switched reversibly. A further discussion of a fabrication of the means as shown in fig. 7-10 is omitted here, as it will in part be well-known to persons skilled in the art and in part is disclosed in the above-mentioned Norwegian patent application and the references cited therein and whereto reference in that connection can generally be made.

Please amend the paragraph on page 30, line 26 as follows:

Now ~~shall~~ transistors will be discussed, particularly field-effect transistors (FET) which may be used as active components in the processing unit and/or in the storage unit in the data processing device according to the present invention and generally be used for realizing processors and interfaces as used in the data processing device according to the invention. If a first processor layer is provided adjacent to a silicon substrate, ~~it will of course be nothing against that~~ the processor layer can be realized with devices in the form of integrated circuits and then as monolithic integrated circuits, but the processor layer can ~~possibly~~ also be realized as hybrid integrated circuits. Field-effect transistors based on amorphous inorganic semiconductors and realized in thin-film technology may for instance be integrated in conventional monolithic solutions in a substantially silicon-based technology. An example ~~of the embodiment~~ of thin-film transistors with the active semiconductor material in the form of amorphous Si:H in a 10 nm thick layer (D.B. Thomasson & al., IEEE E1. Dev. Lett., p.117, vol. 18, March 1997) is shown in fig. 11. A gate electrode 21 which may be a metal is provided in a substrate 20. Above this gate electrode an isolating layer 24 in the form of silicon nitride (SiN) is provided and thereabove is the active semiconducting material 23 in the form of amorphous Si:H provided in a 10 nm thick layer. The drain and ~~respectively~~ the source electrodes 22 are provided mutually separated on the active semiconductor material 23. They are made in another metal than

that which was used in the gate electrode 21 ~~23~~. The use of a processor layer P provided directly on the substrate S or adjacent to a processor interface 3 provided on the substrate S makes it as mentioned possible to realize both layers wholly in a conventional semiconductor technology, either in the form of monolithic or hybrid integrated circuits, and if the additional, overlying processor and memory layers wholly are realised in a technology based on substantially organic materials, a hybrid solution for the data processing device according to the invention is obtained.

Please amend the paragraph on page 31, line 19 as follows:

~~It is also~~ Also ~~nothing against that~~ all main layers, that is processor layers, memory layers and interface layers ~~wholly are~~ can be realized in organic thin-film technology. In that connection it shall be convenient to use an organic thin-film transistor as shown in fig. 12 (A. Dodabalapur & al., Appl. Phys. Lett. Pp. 4227-29, vol. 69, December 1996). Here an active semiconductor material in the form of an amorphous organic compound, for instance a polymer or aromatic molecules is used. The gate electrode 21 is provided on a substrate 20 and above the gate electrode is provided an isolator 24 which as well will be made by applying a oxide coating to the surface of the gate electrode, for instance realized by oxidizing the material in the gate electrode surface. The drain and source electrodes 22 are provided over the isolator layer 24 and mutual spaced apart, and above the drain or source electrode is provided a layer 23-2 ~~23~~ of active

organic semiconductor material which also covers the exposed portion of the gate isolator 24. The organic semiconductor material may be a conjugated polymer or aromatic molecules.

Please amend the paragraph on page 32, line 8 as follows:

A field-effect transistor of this kind is disclosed in Norwegian patent application 980224 which hereby are incorporated as reference and which has been assigned to the applicant. As shown in fig. 13, on ~~On~~ a substrate 20 is provided a film 22 of conducting material which constitutes a first electrode in the transistor. Over this film there is provided an isolating material which constitutes a first isolator ~~25~~ 25-1 and thereabove is provided a further conducting material which constitutes a second electrode 21 in the transistor. On this second electrode 21 is provided a second isolator ~~an isolating material 25 which constitutes a second isolator~~ 25-2 in the transistor and above the second isolator 25-2 is provided a film 22' of conducting material which constitutes a third electrode of the transistor. Realized as a field-effect transistor the first and third electrode 22, 22' constitutes a drain electrode and source electrode respectively of the transistor or vice versa. The second electrode 21 constitutes the gate electrode. Both the second and the third electrode 21; 22' and the isolators 25-1, 25-2 are provided on the first electrode 22, such that they over this and the substrate 20 form a vertical step, the extension of which is indicated wit the reference number 26 in fig. 13. Thus, the structure comprised by the

second or third electrode 21 and 22' and the isolators 25-1, 25-2 only covers a part of the substrate 20 and the horizontal extension of the layers which form the vertical step 26 on the first electrode 22 or the substrate may realized in thin-film technology which can be made very small, for instance some ten nanometers. ~~Above the exposed~~ A surface of the gate electrode 21 ~~25 which is included in~~ of the vertical step 26 is provided an isolating material 24 which constitutes the gate isolator of the field-effect transistor. Over the top of the third electrode 22' which for instance may be the source electrode of the transistor, over the vertical step 6 and down to the first electrode 22 which may be the drain electrode of the transistor, is provided a layer 23 of active semiconducting material which may be an amorphous, polycrystalline or microcrystalline, inorganic or organic semiconducting material.

Please amend the paragraph on page 33, line 1 as follows:

The gate electrode 21 ~~25~~ is isolated against the active semiconducting material 23 by the gate isolator 24, such that charge injection is prevented. A substantially vertical transistor channel 23' is defined in the active semiconducting material 23 and extends between the source and drain electrodes 22, 22' and substantially adjacent to the vertical step 26 as shown. It is optional whether the first electrode 22 and the third electrode 22' respectively shall be the drain electrode or source electrode. The transistor effect will either be given by a depletion mode or an enrichment mode, depending on the gate

potential. - In regard of the fabrication of this field-effect transistor in thin-film technology, reference shall be made to the patent application cited. The field-effect transistor as realized in thin-film technology shall in the vertical direction have a dimension which wholly are compatible with thickness of the processor layer or the memory layer realized in thin-film technology for use in the data processing device according to the invention, but shall have a far smaller horizontal extension than for instance the thin-film transistor shown in fig. 12 and hence furnish a higher device density in a layer in question. - A further field-effect transistor with the MIS structure realized thin-film technology is disclosed in US patent No. 5347144 (Garnier et al.) which hereby is incorporated as reference, and which has been assigned to the applicant. The MISFET shown therein realized in thin-film technology may be used as a switching or amplifying device in the data storage device according to the present invention. This transistor has a thin semiconducting layer between a source electrode and a drain electrode. The semiconductor layer contacts a surface of a thin film of isolating material which by its other surface contacts a conducting gate electrode. The semiconducting material itself comprises at least one conjugated organic compound with a determined molecular weight. The thin film of isolating material is made in an isolating organic polymer which can have a dielectric constant of at least 5.

Please amend the paragraph on page 34, line 17 as follows:

In the present invention the separate main layer, be it a processor layer P or a memory layer M, may be built up by sublayers which shall be provided with different properties before they are joined into a main layer. In a memory may for instance the memory material be provided in a central sublayer and surrounded by separate electrode layers, and there may between the separate sublayers be provided separate isolating layers, such this for instance is evident from fig. 7g. Correspondingly can for instance an active device such as transistor in fig. 12 be built up by depositing sublayers 20, 21, 22, 23 with determined properties: It is, however, thinkable that the transistor structure similar to the one in fig. 12 can be realized in one and the same organic material, as the separate sublayers are processed separately before joining by irradiation with for instance light, such that each of sublayer patterned and unpatterned obtains the desired electrical property which shall enter into the realization of a field-effect transistor in thin-film technology. This is to say that a first sublayer could ~~must~~ be an isolator, a second sublayer a conductor, a third sublayer a semiconductor, a fourth sublayer an isolator and finally a fifth sublayer once again an electrical conductor. For use in the present invention, whether it concerns the memory unit or the processor unit it is also desired to employ active devices, for instance the transistors mentioned, wholly realized in organic material, e.g. polymers. Similarly it is of interest to among other to generate

integrated circuits wholly realized in the form of thin-film polymers. As mentioned above, among others Garnier & al. has developed and patented a MIS field-effect transistor which substantially is wholly realized in polymer technology. Generally it is of interest be able to realize organic field-effect transistors in thin-film technology which simultaneously allows integration of the devices.

Please amend the paragraph on page 35, line 25 as follows:

Fig. 14 shows a MISFET according to D.M. de Leeuw & al. Here doped polyaniline PANI is deposited as a thin film 22 on a polyimide substrate 20. After exposure to UV light through suitable mask isolating structures 25 is formed in the otherwise conducting PANI film 22 ~~23~~. The still conducting areas 22 in the PANI film define respectively source and drain electrode in a MISFET transistor. The PANI film ~~25~~ 22 need not be thicker than 200 nm and comparable with the thickness of the polyimide substrate 20. Above the PANI film 22 a further layer 23 is deposited in the form of polythienylene vinylene or PTV which is an organic semiconducting material. The PTV layer 23 is typically 50 nm thick and may be deposited by known film deposition technologies. The semiconducting PTV film determines substantially the electrical parameters of the MISFET transistor as shown in fig. 14. Over the PTV layer is now deposited a 250 nm thick layer 24 of polyvinyl phenol (PVP), for instance by spin deposition. This PVP layer 24 forms the gate isolator of the field-effect transistor and is opaque to UV radiation and

visible light. Another PANI film 21 is deposited on the top of the PVP layer 24 and once again patterned by irradiation with ultraviolet light, such that isolating structure 25 as shown in fig. 14, are formed. The area 21 is still electrical conducting and forms the gate electrode of the MISFET structure.

Please amend the paragraph on page 37, line 14 as follows:

~~For the purpose of the present invention it is, however~~ However, it is particularly desirable to apply materials which makes it possible to realize the sublayers in the data processing device ~~according~~ to the ~~invention~~ with a well-defined mode and degree of electrical conduction in the production process and before the joining of the sublayers according to the intended function into processor layers P or memory layers M or combination MP thereof. Such materials shall in the following in generally be denoted as convertible materials CM, as the conversion of the electronic properties of the materials may take place reversibly or irreversibly under the influence of radiation, including both photon radiation and particle radiation, heat or electrical fields. By a spatial modulation of the radiation or the electrical fields the material may be patterned, as the desired conversion of the electronic properties will be dependent on the energy supplied or the field strength applied. This is described in more detail in the above-mentioned Norwegian patent application 980385. In contrast to the above-mentioned PANI film it will be preferred that the materials initially are in a dielectric or electric non-conducting state. Where the material CM is not

influenced by the electric fields or light, it will of course retain its dielectric properties and form an isolator, while it in influenced areas depending of the degree of conversion may appear with electrical semiconducting or conducting properties. Areas in the conducting film may hence in the fabrication process stably be provided with a determined degree and mode of electrical conductivity, such that they for the purpose appear as electrical conducting and may be used for forming electrodes and current paths in the separate sublayer, or as semiconducting and forming the active material of diodes and transistors. Used as a memory material the conversion further shall be reversible, such that the material CM forms a bistable electrical switch and makes possible electrically addressable and erasable memories of the above-mentioned kind, cf. the discussion in connection with a memory shown in fig. 7a-7h. The material CM will typically be an organic material, for instance molecules, oligomers and polymers which transfers from an initial first state to a second state under influence of light in a determined frequence range. It is of course to be understood that transition between first state and the second state shall be characterized by a change in degree and mode of the electrical conductivity.

Please amend the paragraph on page 38, line 11 as follows:

As examples of materials which may transition ~~transfer~~ from isolating to conducting state by an irradiation with light, different conjugated polymers may be mentioned, where it is simultaneously used ~~exposure~~ to expose a suitable

dopant in the form of gas or liquid or polyphenylene vinylene (PPV) precursors impregnated with dyes with a strong frequency-selective absorption of light which causes them to be converted into a conjugated polymer by the irradiation. Further ~~may~~ a 2,5-dimetoxyphenylene derivative of PPV (DMEO-PPV) ~~transfer~~ may transition from isolating to semiconducting state by an elimination reaction of polyelectrolyte films formed thereof. It will then be formed a fully conjugated chain by radiation with laser light. ~~To persons skilled in the art a~~ A large number of such organic or polymer-based materials is well-known. ~~and mentioned in the literature, and there shall again be referred to the above-mentioned Norwegian patent application and the references cited therein, among other with a description of organic based thin-film transistors.~~ Semiconducting PPV may be formed by a sulphonium salt precursor by ion irradiation at 1000 kV Ne^+.

Please amend the paragraph on page 38, line 27 as follows:

Fig. 15 shows a forward-biased pn junction diode with conducting and semiconducting structures generated by the method according to the invention and realized in thin-film technology with ~~four~~ sublayers SS1-SS6. The layers SS3 and SS4 contain the active semiconducting material provided between the electrodes 29 in respectively the sublayers SS2 and SS5. The active material 23' in the sublayer SS3 is an n-doped semiconductor, while the adjacent active material 23 in the sublayer SS4 is p-doped semiconductor. The electrodes 29 in

the layers SS2 and SS5 are ~~contacted~~ connected by horizontal electrical conducting structures or conducting paths 27 in layers SS1 and SS6. The separate layer in the diode structure in fig. 15 has typically a thickness of about 100 nm such that the whole structure forms a multilayer structure with a thickness less than 1 μm. The horizontal extension of the area of the diode structure will be determined by the method for generating conducting semiconducting structures, but by using for instance visible or ultraviolet light, an extension of less than 1 μm may be obtained.

Please amend the paragraph on page 39, line 24 as follows:

The MOSFET structure in fig. 16 may now be used in logic gates, for instance a logic inverter in CMOS technology as shown in fig. 17a. An inverter of this kind is formed by parallel connection of the drain and source electrode in respectively an NMOSFET and a PMOSFET. For this purpose a vertical conducting structure 28 is generated and passes through all sublayers SS1-SS11 and connects the electrodes 22'. The output signal from the inverter is conveyed on this conducting structure 28 to a horizontal conducting structure 27 at left in the figure. The gate electrodes 21 of the MOSFETs receive the input signal via the horizontal conducting structure 27 in the sublayer SS6 at right in the figure. As gate electrodes 22 of course is at the same potential, they could be common for the inverter as shown in fig. 17b whose MOSFETs in the figure are shown realized in a back-to-back arrangement. Also the vertical electrical

conducting structures in the sublayers SS1 and SS11 could ~~as shown in fig. 17b~~ be moved to the sublayers SS2 and SS10. The inverter structure of fig. 17~~b~~a could then be formed with seven and not eleven sub-layers as shown in fig. 17a. The thickness of all sublayers will then be less than 1 μm, typically realized with about a thickness of about 0.7 μm, while the horizontal extension of the inverter will have the same dimensions as stated above in connection with the discussion of the MOSFET structure in the figure 16.

Please amend the paragraph on page 41, line 10 as follows:

~~Purely practically the~~ The AND gate can easily be implemented in thin-film technology as shown in figs. 19a-19d and with the use of MOSFET structures corresponding to that shown in fig. 7. Figs. 9a-19d show the AND gate wholly realized in thin-film technology and with the active and passive devices provided in four sublayers SS1, SS3-SS5. The first sublayer SS1 (fig. 19a) contains the gate electrodes g_1-g_6 where the subscript points to the corresponding subscript for the MOSFETs Q_1-Q_6 in fig. 18. The inputs A and B are conveyed to respectively the gate electrodes g_1, g_3 and g_2, g_4 and via horizontal conducting structures or current paths 27. Correspondingly the gate electrodes g_5, g_6 in the inverter are connected with a horizontal current path 27. A vertical electrical conducting structure is denoted 28, the symbol Δ indicating that it extends upwards in vertical direction from the sublayer SS1. In fig. 19b the symbols Δ and ∇ likewise indicate that the vertical conductor structure 28 in the layer SS3

extends vertically through this layer and on both sides thereof. The vertical layer SS3 comprises areas with active semiconductor material b_1-b_6 which are assigned to and register with the corresponding gate electrodes g_1-g_6 in the layer SS1. ~~It is to be remarked~~ Note that a layer SS2 ~~exclusively, apart from the vertical conductor structure 28 which also extends through this sublayer on both sides thereof, consists~~ is made of dielectric material which forms a common gate isolator for the MOSFETs Q_1-Q_6 which realize the AND gate. - The layer SS2 is, of course, located between SS1 and SS3, but has been excluded from the drawing. - The layer SS4 (fig. 19c) is provided above and adjacent to the layer SS3 and comprises respectively the source electrodes s_1-s_6 and the drain electrodes b_1-b_6 for the corresponding MOSFETs Q_1-Q_6. The active semiconductor material d_1-d_6 which is located in the layer SS3 is here indicated by stitched lines. The vertical current path 28 also extends also through the layer SS4 and to both sides thereof and contacts a horizontal current path 27 in the sublayer SS5 as shown in fig. 14d. This horizontal current path 27~~d~~ corresponds to the connection between the drain electrodes d_2 and d_3 for the corresponding MOSFETs Q_2, Q_3 and is additionally also connected with the drain electrode d_1 on Q_1. Another horizontal current path 27 realizes the serial connection between the source electrode s_1 on Q_3 and the drain electrode d_4 on Q_4. The source electrodes s_4 and s_6 are grounded on further horizontal conducting structures 27, while horizontal conducting structure 27 farthest to

right in the layer SS5 is supplied with a voltage V_{dd} and connects the source electrodes s_1, s_2, s_5 on respectively Q_1, Q_2, Q_5. A further horizontal current path 27 uppermost in fig. 19d forms the parallel connection between the drain electrodes d_5,d_6 on Q_5, Q_6 and the output line, denoted with X. The inverted output signal X from the NAND gate consisting of Q_1, Q_2, Q_3, Q_4 is conveyed on the vertical current path 28. Fig. 20 shows schematically how the layers in fig. 19 appear in stacked configuration, the layer SS2 with the gate isolator here being included. For the sake of clarity, however, the stack is shown exploded in its separate sublayers SS1-SS5, but with correct registration and the course of the vertical current path 28 through all sublayers is indicated by the stitched line. With the gate electrode layer SS1-SS5 provided on an underlying, not shown dielectric layer, the total AND structure as shown in fig. 11 may have a thickness of 0.75 μm and an area of about 100 μm^2 (12·8 μm^2). The volume of the structure will hence be about 75 μm^3. With conservative spatial resolution this implies that about 10 000 logic gates of this kind may be realized on an area of 1 mm^2 and with a thickness well below 1 μm. Correspondingly scaled the length of the current paths 27, 28 together becomes 60 μm.